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Innovative Silicon Inc. Creates Technology Advisory Board

Team consists of leading memory and SOI industry experts, Dr. Jean-Pierre Colinge, Dr. Michel J. Declercq, Dr. Richard C. Foss, Dr. Carlos Mazure, and Mark McDermott

SANTA CLARA, Calif., May 4, 2006 — Innovative Silicon Inc. (ISi), the developer of Z-RAM® high density memory IP, today announced that it has recruited semiconductor memory and Silicon on Insulator (SOI) luminaries Dr. Jean-Pierre Colinge, Dr. Michel J. Declercq, Dr. Richard C. Foss, Dr. Carlos Mazure, and Mark McDermott to participate in the company's newly formed Technology Advisory Board (TAB). The new board members will help ISi as it ramps up sales and continues the development of its Z-RAM memory IP, which is five times denser than embedded SRAM and twice as dense as emerging embedded DRAM.

"ISi is a forerunner in memory technology developments and we attribute our success to the fact that our company's founders, Drs. Pierre Fazan and Serguei Okhonin, had a clear understanding of the industry's need for ultra-dense embedded memory when they created our Z-RAM memory technology," said Mark-Eric Jones, CEO of ISi. "The makeup of our TAB gives us access to an excellent cross section of experts who have their fingers on the pulse of the industry. Moreover, as our advisors are the most renowned and respected talent in both memory and SOI technology developments, they can provide us with valuable insight into the evolving requirements of system on chip (SoC) and microprocessor developers as they scale their designs to 65nm and smaller process geometries."

The advisors will help ISi with the following:

- Identify technology trends and issues that are relevant to the company's business direction
- Provide perspective on today's memory and semiconductor challenges
- Prioritize issues and provide input on possible solutions
- Provide contacts and references for specific technology issues
- Facilitate access to industry committees and user groups
- Review and assess the company's roadmap

The TAB Team

Dr. Jean-Pierre Colinge, a renowned pioneer in SOI devices, is currently a professor at the University of California, Davis. Previously, the IEEE Fellow was professor at the Université Catholique de Louvain, leading a research team in the field of SOI technology, and also with IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. Dr. Colinge also worked at Hewlett-Packard Laboratories, Palo Alto, Calif., investigating thin-film SOI CMOS and bulk bipolar technologies for high-speed digital applications, and at CNET, Meylan, France, where he developed new silicon-on-insulator and 3D integration technologies using laser recrystallization. Dr. Colinge has published over 270 scientific papers and three books on the field of SOI, as well as two books on semiconductor device physics.

Dr. Michel J. Declercq, an IEEE Fellow and recognized European Commission expert on scientific research programs in IT, brings extensive SOI design expertise to ISi. He joined the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1985, where he is currently Professor, Dean of the School of Engineering, and Director of the Electronics Laboratory. His research activities are related to mixed analog-digital IC design and design methodologies. His primary research areas include low-power/low-voltage circuits, high-frequency circuits for telecommunications, MEMS and RF-MEMS, SOI technology and circuits, high-voltage circuits and nano-electronics.

Dr. Richard C. Foss, co-founder and former CEO of MOSAID, brings memory design and extensive IP and patent knowledge to ISi. Prior to MOSAID, he held various positions including the head of design at Microsystems International – where he worked on a trend-setting 4K DRAM – and at Plessey, where he led a pioneering circuit design group with many creative successes in linear ICs, high speed counters, and early MOS devices. Also an IEEE Fellow, Dr. Foss has published numerous papers on semiconductor design.

Dr. Carlos Mazure, chief technical officer of Soitec, has managed the company's strategic Advanced Technology Development organization since 2001. He drives the identification and development of next-generation engineered substrates for the semiconductor industry, as well as the emerging applications effort, defining future business directions. He works closely with Soitec's customers to help support and open new substrate engineering applications. Prior to joining Soitec, Dr. Mazure served as director of business development at Infineon Technologies, was involved with the IBM/Infineon DRAM Development Alliance in East Fishkill, New York, and worked on SOI and BiCMOS high performance SRAM and technology development at Motorola Semiconductor in Austin, Texas. Dr. Mazure holds two doctorates in physics, has authored over 150 technical papers and holds more than 70 patents worldwide.

Mark McDermott is a serial entrepreneur, having co-founded six companies during his 29-year career. He has led engineering teams in the development of PowerPC processors and Intel x86 processors and has 19 patents in the area of microprocessor design and test. Currently, he is VP of Engineering at Coherent Logix, Inc. and Principal and General Partner in the Silicon Web Group, a consulting firm focused on EDA startups. McDermott also holds the post of Adjunct Assistant Professor at the University of Texas where he teaches graduate level courses in VLSI design, system-on-chip design and technical entrepreneurship.

Z-RAM Background

ISi's Z-RAM technology was created to solve one of the biggest challenges for SOC designers: how to shrink die sizes when memory dominates chip area and cost. Since ISi's Z-RAM (one transistor, zero-capacitor) technology is five times smaller than embedded SRAM and up to twice as dense as emerging embedded DRAM technologies, Z-RAM enables IC manufacturers to cut their die cost in half while getting the performance and power advantages that SOI delivers over bulk CMOS technologies.

About Innovative Silicon

Incorporated in 2002, Innovative Silicon was founded to develop and commercialize Floating Body effect memory for SoC/MPU products used in diverse applications including microprocessors, handheld computers, games consoles, cellular communications devices, and cameras. The company closed its first round of VC funding in 2003, completed its first 90nm megabit Z-RAM memory designs in 2004 and its first 65nm designs in 2005. The company is incorporated in the USA with R&D in Lausanne, Switzerland. For more information see <http://www.z-ram.com>.

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