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## **Innovative Silicon Unveils Z-RAM Memory Technology Breakthroughs at 2008 IEEE International SOI Conference**

*Smallest silicon dynamic memory devices ever reported*

*Largest programming window, significantly improved retention time demonstrated*

**2008 IEEE INTERNATIONAL SOI CONFERENCE, New Paltz, N.Y. — October 9, 2008** — Innovative Silicon, Inc. (ISi), developer of the Z-RAM® zero-capacitor floating body memory technology, demonstrated here that its Z-RAM memory technology continues to show considerable advantages over DRAM implementations and other proposed floating body memory designs. Dr. Mikhail Nagoga, a principal member of ISi's technical staff, presented a paper written by Dr. Serguei Okhonin, chief scientist at ISi, that describes the smallest silicon dynamic memory devices ever reported, with the largest programming window. Separately, Dr. Ammar Nayfeh, a member of ISi's technical staff, presented a paper that discusses improvements in Z-RAM memory retention times and a reduction in leakage current.

In the paper delivered by Nagoga, titled "Ultra-scaled Z-RAM cell," Z-RAM cells based on Multiple-gate SOI MOSFETS (MUGFETs) with gate length down to 50nm and fin width down to 11nm were demonstrated for the first time. Simulations proved that the basic operational principles are effective on Z-RAM cells with gate lengths down to 12.5nm and fin widths of 3nm.

Further analysis also shows that these devices exhibit the largest programming window (margin) ever recorded. Measured as the difference in current between STATE 1 and STATE 0, the programming window of these MUGFETs is close to 22µA.

Okhonin commented, "Even such small devices demonstrate a reliable memory effect, and the experimental data presented in the two papers indicates the excellent scalability of our Z-RAM memory devices. Further, we must remember that the results that we demonstrated today are only achievable in a floating body architecture. We also believe our transistors are not only the smallest silicon dynamic



memory devices ever published, but also the best performing. At equivalent gate lengths, we also demonstrated a several times larger programming window vs. other published data.”

Nayfeh’s paper, co-authored with ISi fellow Dr. Victor Koldyaev and titled, “A Leakage Current Model for SOI based Floating Body Memory that Includes the Poole-Frenkel Effect (PFE),” describes for the first time how the leakage current of SOI based floating body memory has been modeled and compared to experimental Z-RAM data, taking into account oxide/SOI  $D_{it}$  and PFE. The model has enabled the Z-RAM design team to significantly reduce the number of defects per cell, leading to an increase in retention times and a reduction in leakage current.

Jim Feldman Semico president noted, “ISi continues to demonstrate unmatched memory density and performance with its Z-RAM technology. It is also exciting to see the ongoing innovation advancing this floating body implementation.”

### **About Innovative Silicon**

Innovative Silicon, Inc. (ISi) is the inventor and licensor of the Z-RAM® ultra-dense memory technology for stand-alone DRAM and embedded memory applications. Z-RAM is the world’s lowest-cost semiconductor memory technology – simpler to manufacture than DRAM, and a fraction the size of SRAM. ISi and the Z-RAM technology have received numerous industry awards, including the World Economic Forum’s selection of ISi as a 2008 Technology Pioneer, and IEEE Spectrum Magazine’s selection of Z-RAM as the 2007 “Emerging Technology Most Likely to Succeed.” Z-RAM is a “Zero Capacitor,” true single-transistor floating body memory that eliminates the complex capacitor found in today’s DRAM technologies – a fundamental roadblock to Moore’s Law of scaling. Z-RAM provides semiconductor manufacturers a solution for nanoscale manufacturing processes that can dramatically lower semiconductor costs. The Z-RAM memory technology has been licensed by Hynix Semiconductor for use in its DRAM chips, and by AMD for use in microprocessors. Since 2003, the company has closed three funding rounds totaling \$47 million, received over 30 patents on the technology, developed test chips in multiple technologies from 90nm to 32nm, and has established global R&D, engineering and support centers in Europe, Asia and North America. For more information see [www.z-ram.com](http://www.z-ram.com).

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