In Search of a Better DRAM

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In1966, Dr. Robert H. Dennard, a Fellow at the IBM Thomas J. Watson Research Center created the one-transistor DRAM (Dynamic Random Access Memory). In 1970 Intel released the first DRAM chip, a 1K PMOS device. Since that time, the basic DRAM building block has consisted of a single transistor and an increasingly complex capacitor.

The DRAM industry has achieved miracles cramming more and more memory bits onto ever smaller silicon die – and selling it for cents. Currently 1Gbit and even 4Gbit devices are available. Process engineers have performed heroically, especially with respect to the capacitor element, which has become harder and harder to scale, especially as device geometries shrink.

Scaling introduces yet another major problem for the DRAM manufacturers – leakage current. In both the bitcell as well as the supporting circuitry, leakage becomes more significant as CMOS processing nodes progress from 90nm, through 78nm, 50nm and 45nm. Memory chips are already being discussed at 32nm, at which point leakage in traditional designs will grow to become very difficult and prohibitively expensive to counter, and will require new architectures, changes to standard operating specifications and significant process changes.

The problem of scaling and leakage – as well as device size – rests fundamentally with the basic transistor/capacitor building block. While the transistor element is theoretically infinitely scalable – at least for the foreseeable future – the capacitor is not. Capacitors can be fabricated as high stacks or deep trenches. However, if the overall bitcell size shrinks due to increased density or a smaller process node, then the capacitor will have to be made higher or deeper in order to maintain the minimum charge required for reliable operation.

We are fast-approaching the scaling limits for the capacitor element, and it is clearly time for a new approach. The DRAM industry – including producers and consumers – needs a better DRAM.

Transistors that are fabricated on Silicon on Insulator (SOI) substrates exhibit what is termed the "floating body effect" (FBE), which leads to the accumulation of charge in the body of the transistor. In the past, the floating body effect was regarded as a parasitic nuisance of SOI transistors.

Since the discovery of this effect, there have been many attempts to manipulate and enhance the body charge so that it can be used to reliably store a logical 'state' and function as a memory element. The objective is a memory bit cell that comprises only a single transistor – fundamentally the simplest and most scalable of all semiconductor devices.

Many companies (Intel, Toshiba, IBM, STMicroelectronics, and others) have investigated floating body memories. However, Innovative Silicon, Inc. (ISi) – a memory technology company founded in 2002 – recognized that a conventional approach to creating a floating body memory was unlikely to lead to a manufacturable product. Instead, the company stepped back from product development and refocused its efforts on researching some of the more fundamental aspects of floating body memories. Those efforts have resulted in Z-RAM®, a revolutionary new type of floating body memory.

Although functionally similar to other floating body memories, Z-RAM improves upon them by storing a significantly larger charge in a smaller transistor. This increased amount of charge greatly improves the amount of time the memory can retain its state, as well as the signal margin between a '1' and a '0' state.

Other improvements include faster read and write speeds while simultaneously reducing write power.

Principle of operation

Previous approaches to floating body memories have used the MOS transistor to pass current and create charge in the body using impact ionization. Although memory functionality can be demonstrated, the amount of charge created is insufficient to create a robust and manufacturable memory device.

Z-RAM utilizes the bipolar transistor intrinsic in the SOI MOS structure to create charge (Figure 1). This approach allows a much larger charge to be created and stored due to the increased capacitance of the memory cell.

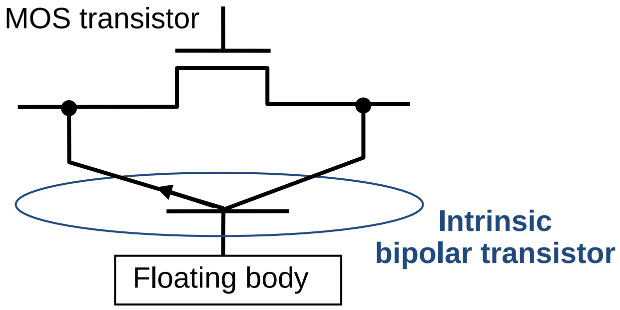

Fig. 1 Intrinsic bipolar transistor

If we consider an n-channel device, the N+ source, the P-type body and the N+ drain form the emitter, base and collector respectively of an NPN bipolar transistor. The body of the MOS transistor is the base of the bipolar transistor and is used as a storage node.

To write a ‘1’ into a Z-RAM memory cell, the intrinsic bipolar transistor is triggered, causing current to flow throughout the transistor body. This differs significantly from MOS behavior where current flows only at the interface. Charge collects at the interface due to the slight bias at the gate. The impact ionization effect used to create an excess of majority carriers in the floating body is more efficient in this bipolar bit cell structure, charging the body quickly, resulting in a very rapid write time (see Figure 2).

Z-RAM memory is read using a similar mechanism which senses the bipolar current through the transistor (Figure 3).

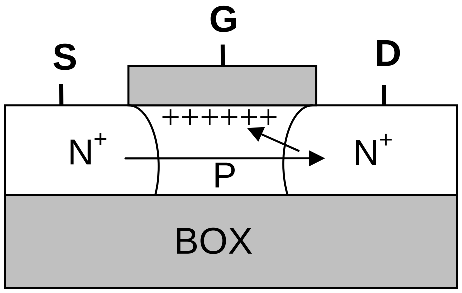

Fig. 2 Writing ‘1’ in Z-RAM

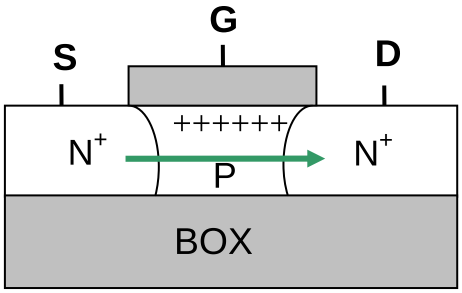

Fig. 3 Reading ‘1’ in Z-RAM

Z-RAM write current is close in value to the read current (Figure 4), and the latch-up characteristic of the intrinsic bipolar causes the behavior of the memory cell to appear nearly digital.

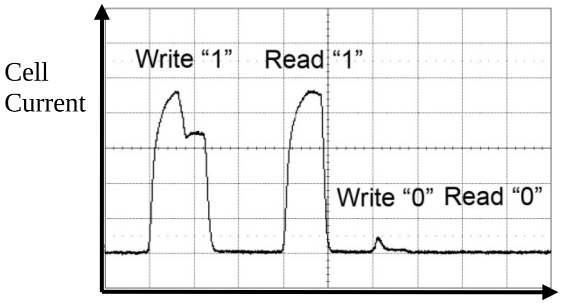

Fig. 4 Z-RAM cell current during operation

The signal margins of the Z-RAM cell are superior to other floating body memories due to the large current gain available from the bipolar device. In Figures 5 and 6 below, Z-RAM naturally provides high margins in comparison to floating body DRAM.

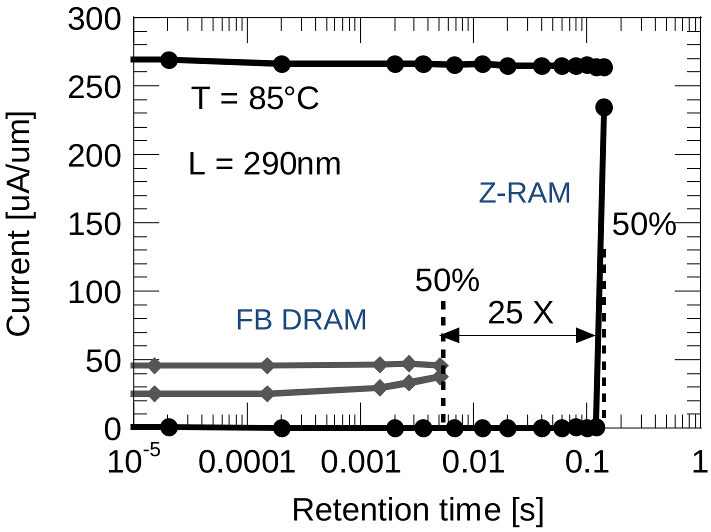

Fig. 5 Floating body DRAM vs. Z-RAM retention and current programming window measured on the same transistor

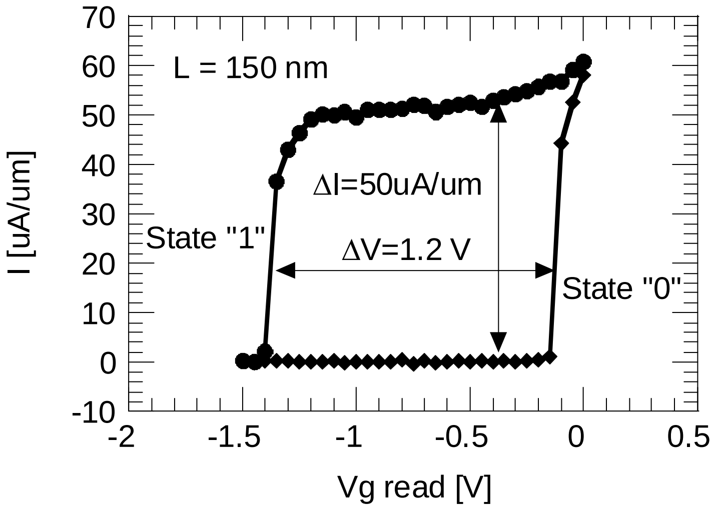

Fig. 6 Z-RAM current and voltage programming window

Scalability

When implemented with conventional planar transistors, the large Z-RAM voltage margin helps to mitigate the negative effects of process fluctuations, which become increasingly significant at smaller process geometries. And perhaps just as importantly, Z-RAM is compatible with advanced, non-planar devices such as FinFET, multi-gate FET, and gate-all-around FET.

In a FinFET or Tri-Gate based Z-RAM, the charge accumulates under the transistor gate and the current flows in the middle of the fin structure. The charge is stored throughout the fin, permitting excellent control of the bipolar current.

Whether fabricated on planar or 3D structures, Z-RAM floating body memory will continue to scale with the technology.

Conclusion

Today, the need for a new approach to manufacturing DRAM is widely recognized. Floating body memories are being widely investigated and appear to be a compelling replacement for conventional DRAM. ISi has implemented a major improvement to a standard floating body memory with its use of the intrinsic bipolar transistor allowing it to store a significantly increased charge. Moreover, ISi is very far along in the development of a complete working memory, having already demonstrated working memory arrays.

But the most compelling argument lies in what companies who manufacture memory and related devices are doing. Both Hynix, a major worldwide manufacturer of standalone DRAM, and AMD, who embed substantial amounts of memory in their microprocessors, have licensed Z-RAM, to incorporate into their products.