



Press Contacts:

Eileen Elam
KJ Communications (in the U.S. for ISi)
Tel: +1 408 927-7753
eileen@kjcompr.com

Nick Foot
Billings PR (in Europe for ISi)
Tel: +44 1491 636393
nick.foot@billings-europe.com

MEDIA ADVISORY

INNOVATIVE SILICON TO PRESENT FLOATING BODY MEMORY ARRAY RESULTS AT ISSCC

***Company demonstrates Z-RAM® memory operation in high-speed cache
application on leading-edge process node***

SANTA CLARA, Calif., — February 3, 2009 — [Innovative Silicon, Inc.](http://www.innovative-silicon.com) (ISi), developer of the Z-RAM® zero-capacitor floating body memory technology today announced the upcoming delivery of a presentation titled “[A 2ns-Read-Latency 4MB Embedded Floating Body Memory Macro in 45nm SOI Technology](#)” in collaboration with AMD at the International Solid State Circuits Conference (ISSCC). The findings, highlighted in a co-authored paper, result from collaborative efforts between the two companies over the past three years to bring-up Z-RAM memory on a contemporary SOI process technology. Unlike ISi’s focus on developing Z-RAM memory as a stand-alone DRAM replacement, this paper will demonstrate Z-RAM memory implemented as an ultra-dense, multi-megabit, on-chip cache memory which occupies approximately 60 percent less area than conventional cache memories. The presented results demonstrate the fastest floating-body memory array reported, and the most advanced technology node reported.

Where: San Francisco Marriott Hotel
55 Fourth Street
San Francisco, CA

When: Session 27.3 on Wednesday, February 11 from 2:30 – 3:00 p.m.

ISi’s Anant Singh will present the paper, which was also written with the assistance of: Philippe Bauser, Paul de Champs, Hamid Daghighian, Dave Fisch, Philippe Graber and Michel Bron of ISi, and Michael



Ciraula, Don Weiss, and John Wu from AMD. The paper describes an embedded memory macro developed for high-performance microprocessors using a single-transistor floating-body cell. Eight 4Mb macros were incorporated on a test chip fabricated in a 45nm SOI logic process. Silicon measurements confirmed a 2ns read latency with a memory-macro operating window of 0.6V.

About ISSCC

The [International Solid-State Circuits Conference](#) is the foremost forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

About Innovative Silicon

Innovative Silicon, Inc. (ISi) is the inventor and licensor of the Z-RAM® ultra-dense memory technology for stand-alone DRAM memory applications. Simpler to manufacture than DRAM, Z-RAM is the world's lowest-cost semiconductor memory technology. ISi and the Z-RAM technology have received numerous industry awards, including the World Economic Forum's selection of ISi as a 2008 Technology Pioneer, and IEEE Spectrum Magazine's selection of Z-RAM as the 2007 "Emerging Technology Most Likely to Succeed." Z-RAM is a "Zero Capacitor," true single-transistor floating body memory that eliminates the complex capacitor found in today's DRAM technologies – a fundamental roadblock to Moore's Law of scaling. Z-RAM provides semiconductor manufacturers a solution for nanoscale manufacturing processes that can dramatically lower semiconductor costs. The Z-RAM memory technology has been licensed by Hynix Semiconductor for use in its DRAM chips, and by AMD for use in microprocessors. Since 2003, the company has closed three funding rounds totaling \$47 million, received dozens of patents on the technology, developed test chips in multiple technologies from 90nm to 32nm, and has established global R&D, engineering and support centers in Europe, Asia and North America. For more information see www.z-ram.com.

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