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**ISi CEO Mark-Eric Jones on Consumer Panel
at the IET/FSA Semiconductor Exec Form**

CEO to highlight how ultra-dense Z-RAM technology can reduce die size, cut power, increase performance, and slash the cost of consumer SoCs

Santa Clara, Calif., May 5, 2006 -- Mark-Eric Jones, CEO of Innovative Silicon Inc. (ISi), the developer of Z-RAM[®] (Zero Capacitor DRAM) high density memory IP, will present on the Consumer Electronics Panel Session at the 2006 FSA Suppliers Expo EUROPE & IET/FSA International Semiconductor Executive Forum to be held on May 9 and 10, 2006 at the Hotel Bayerischer Hof, Munich, Germany.

Mr. Jones will present his views on the exciting opportunities in consumer markets, from the perspective of a company that provides a unique technology enabling IDMs and Fabless companies to work within the tough constraints of markets that will not accept compromises on power consumption, performance or cost.

Aimed at key executives in the semiconductor industry, the IEE organises this annual conference in partnership with the Fabless Semiconductor Association. The conference has a strong financial element and panel subjects include VC funding and market outlooks from analyst companies as well as the Consumer Electronics session, which is scheduled for Tuesday, May 9.

The Consumer Electronics Panel is being moderated by Chris Edwards, Editor of the IEE Electronic Systems & Software Magazine, and will include other panellists from



leading microprocessor and IP companies, such as Anthony Sethill, CEO, Frontier Silicon Limited; Yannick Levy, CEO, DiBcom; and Jon Hudson, Senior VP, CSR.

See www.fsa.org/suppliers_expo/europe2006/ for more information.

About Innovative Silicon

Incorporated in 2002, Innovative Silicon was founded to develop and commercialize Floating Body effect memory for SoC/MPU products used in diverse applications including microprocessors handheld computers, games consoles, cellular communications devices, and cameras. The company completed its first 90nm megabit Z-RAM memory design in 2004 and its first 65nm designs in 2005; verifying that Z-RAM is capable of doubling memory density compared with existing embedded DRAM technology, and achieving five times the density of embedded SRAM. Z-RAM uses a standard SOI logic process with no additional steps or masks. The company closed its first round of VC funding in 2003 and is incorporated in the USA with R&D located in Lausanne, Switzerland.

www.z-ram.com